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(54) Imaging device for imaging radiation

(57) An imaging device for imaging radiation includes an image cell array (16, figure 1). The image cell array includes an array of detector cells 19 which generate charge in response to incident radiation and an array of image cell circuits 20. Each image cell circuit is associated with a respective detector cell. The image cell circuit includes counting circuitry 44 for counting plural radiation hits incident on an associated detector cell, so that counts can be made for each cell in the array individually. The image cell circuit also includes threshold circuitry 42 connected in between each detector and each counting circuit. This receives signals generated in the associated detector cell, the size of which are dependent on the incident radiation energy, and compares these signals with one or more threshold values. The counting circuitry is then connected to the threshold circuitry so that only radiation hits within a predetermined energy range or ranges are counted.

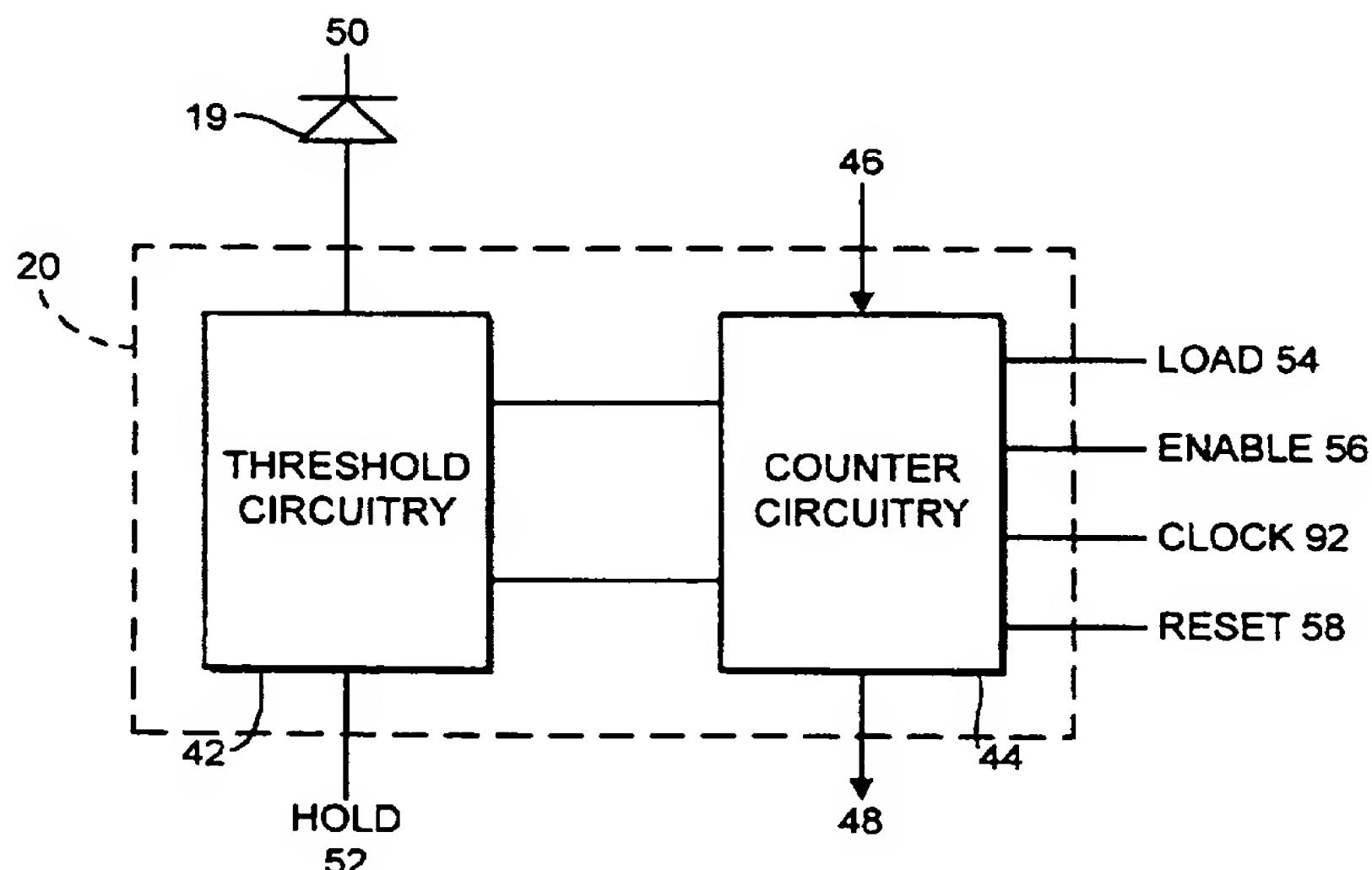
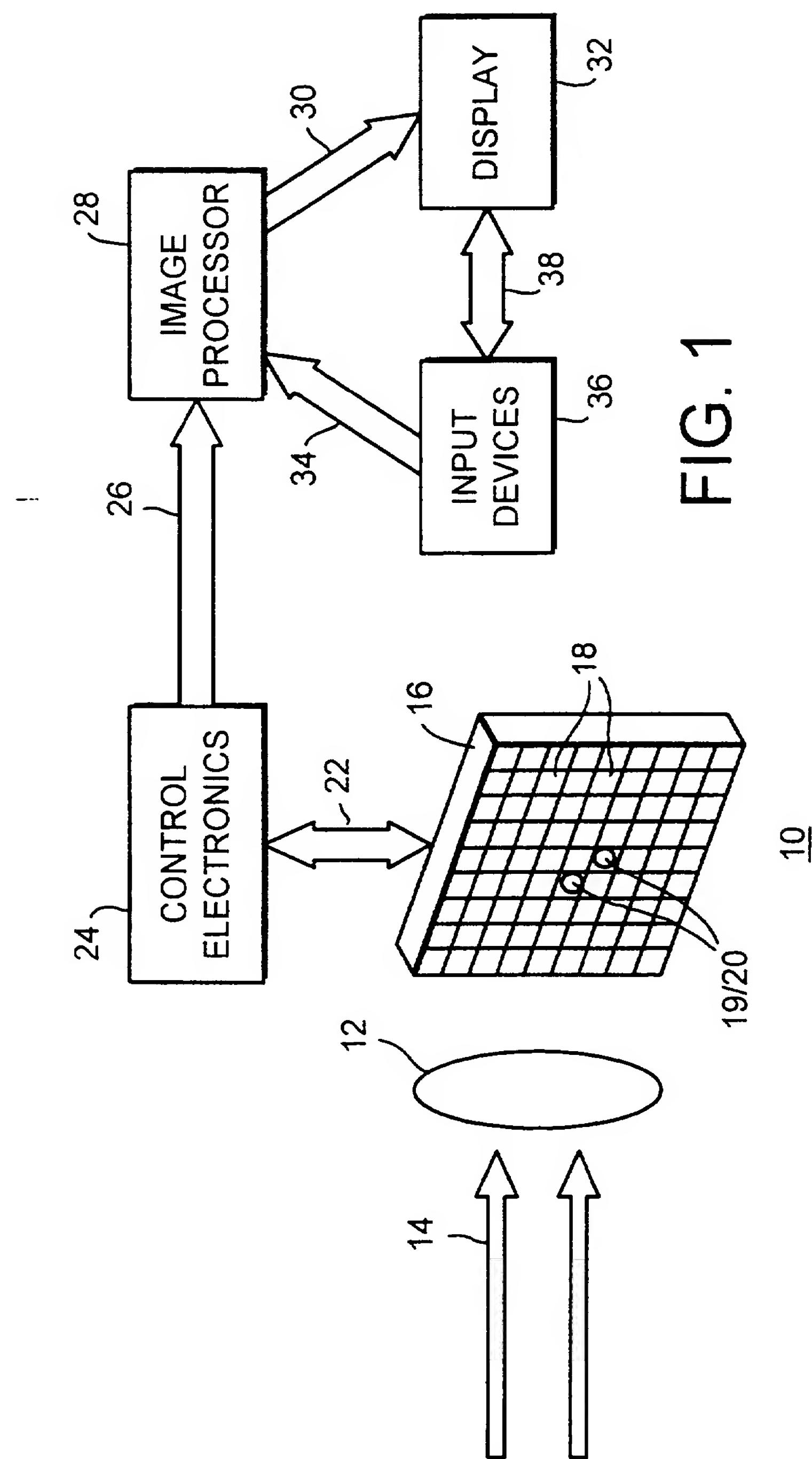


FIG. 3



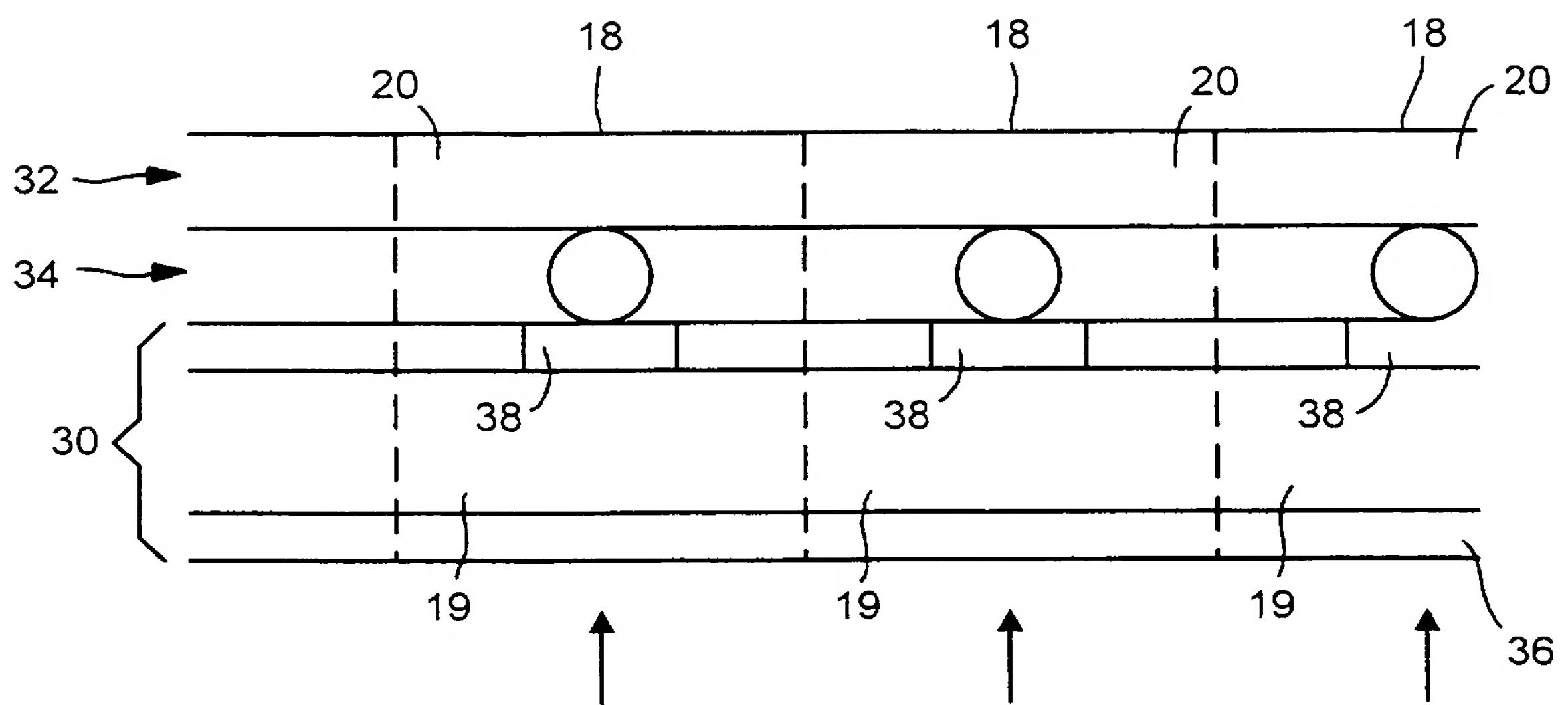


FIG. 2

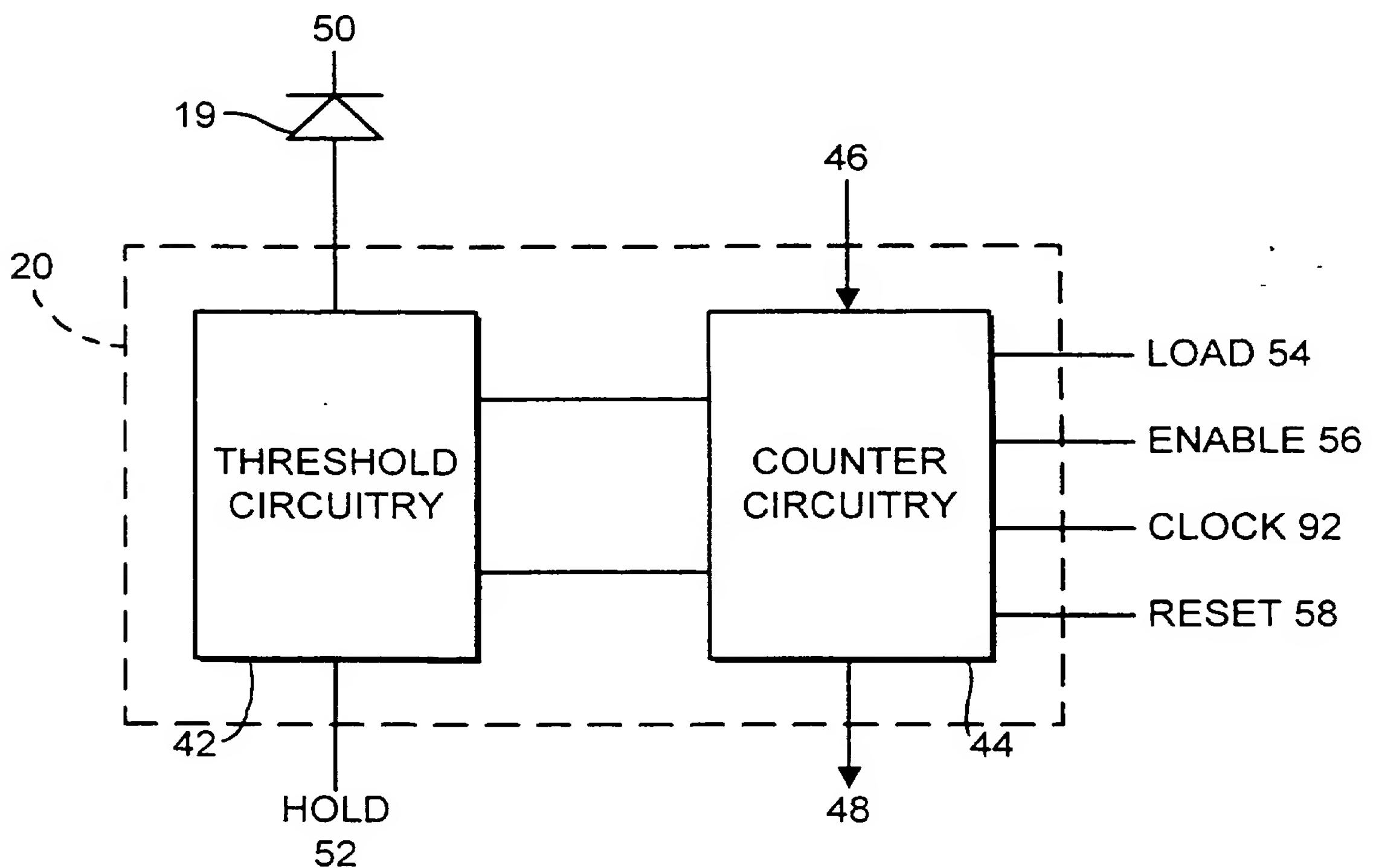


FIG. 3

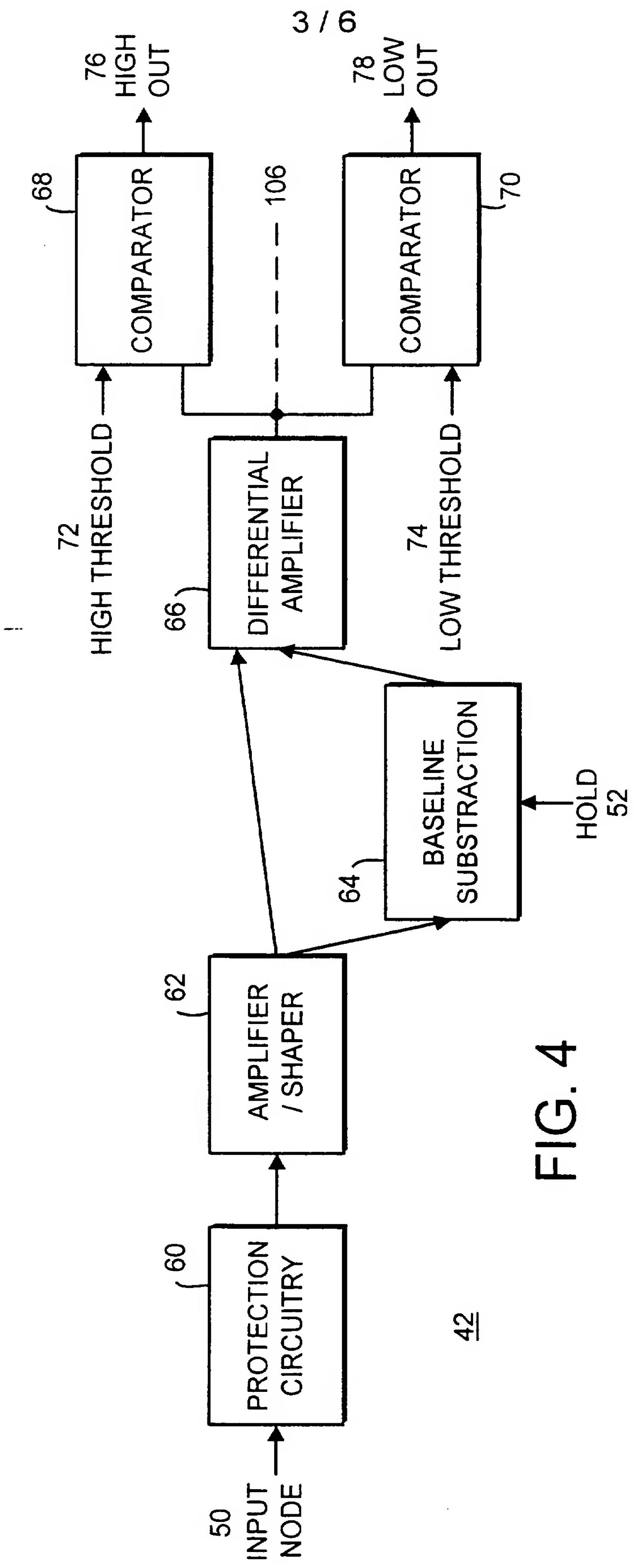


FIG. 4

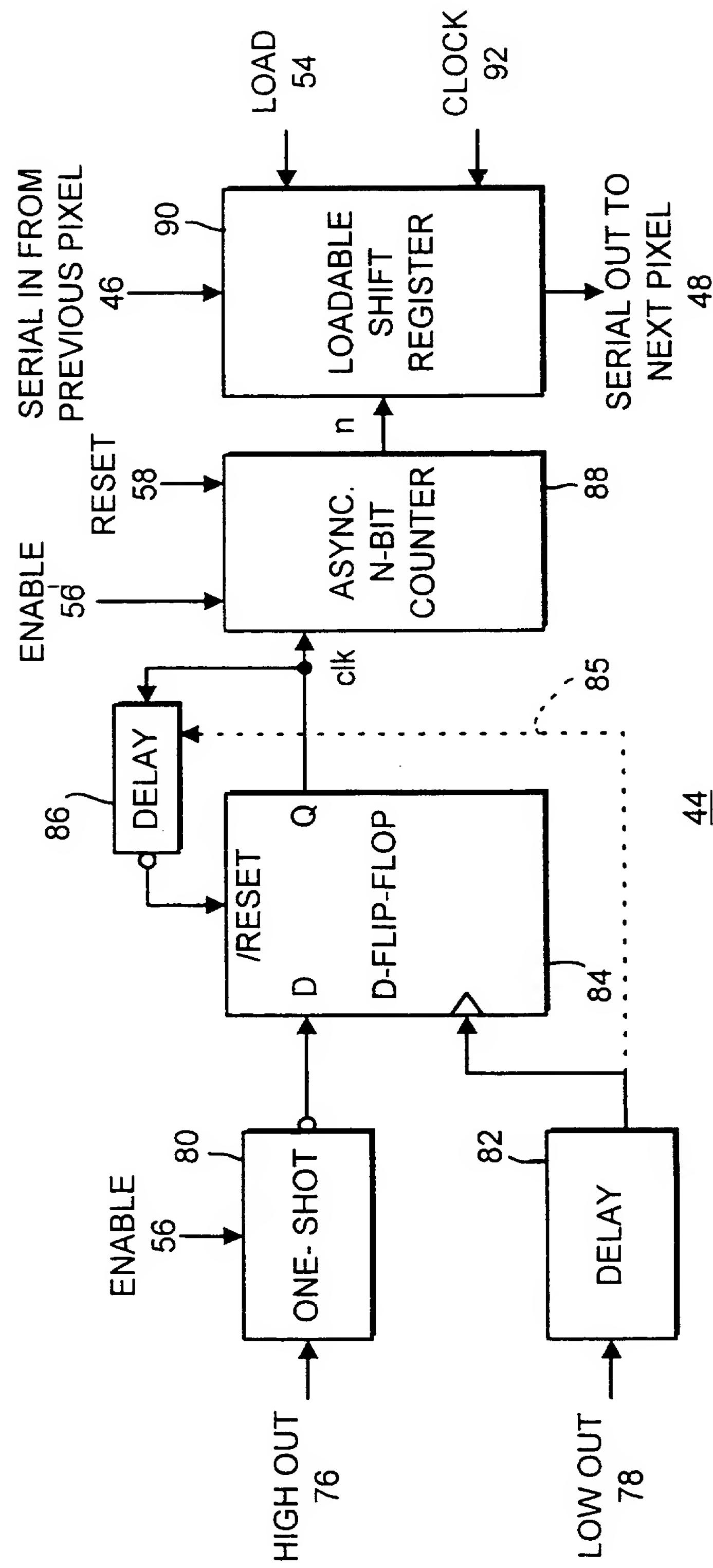


FIG. 5

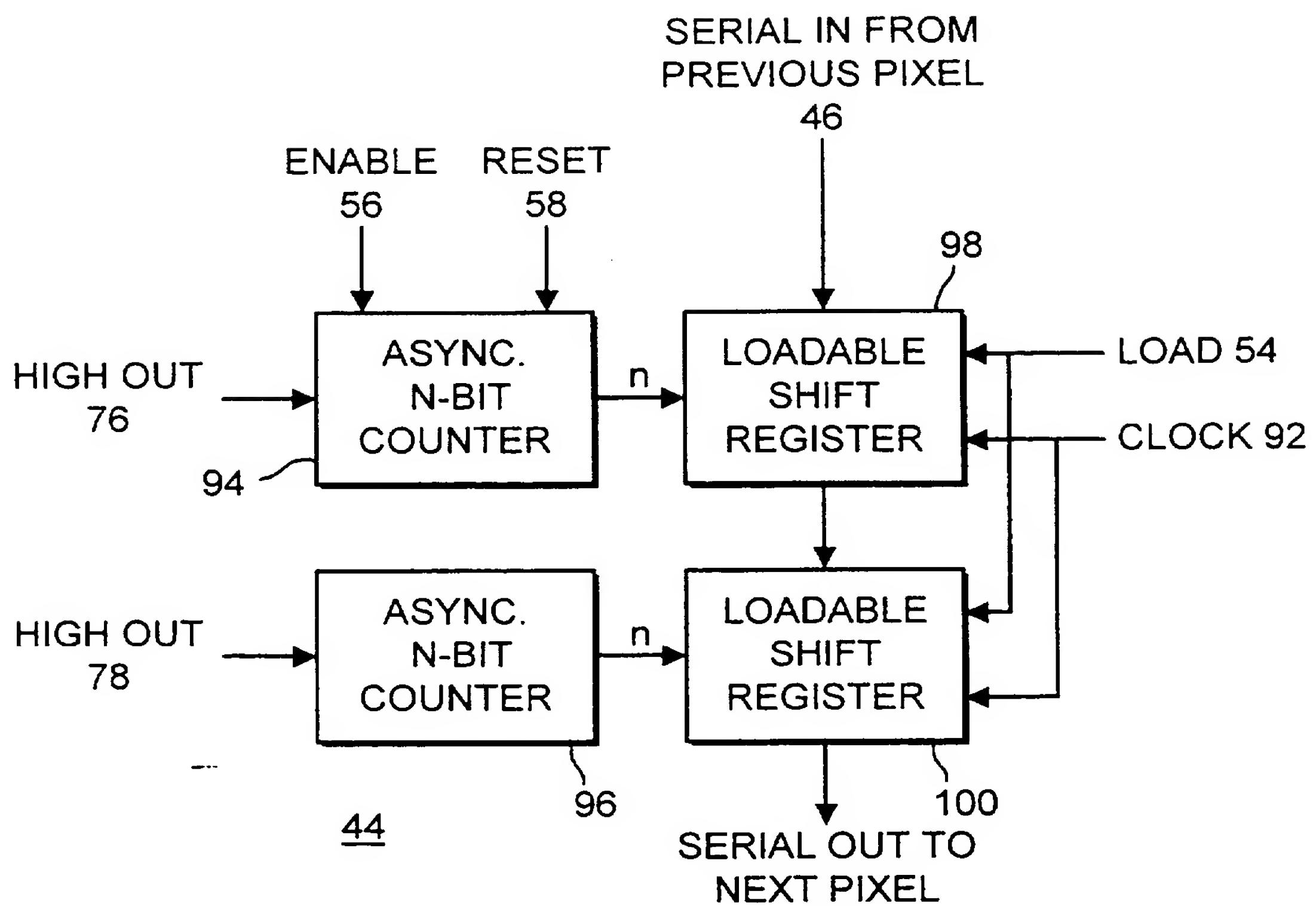


FIG. 6

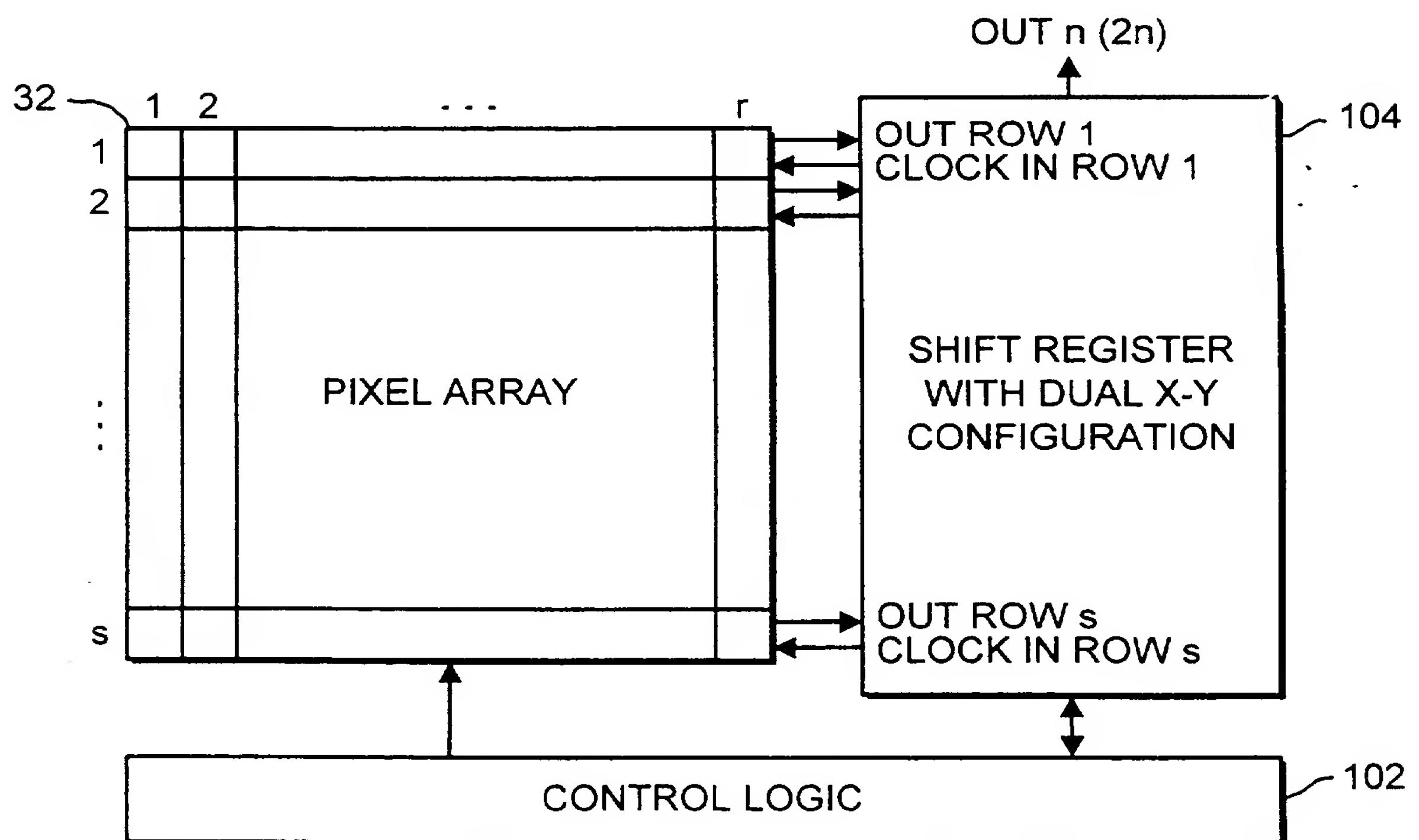
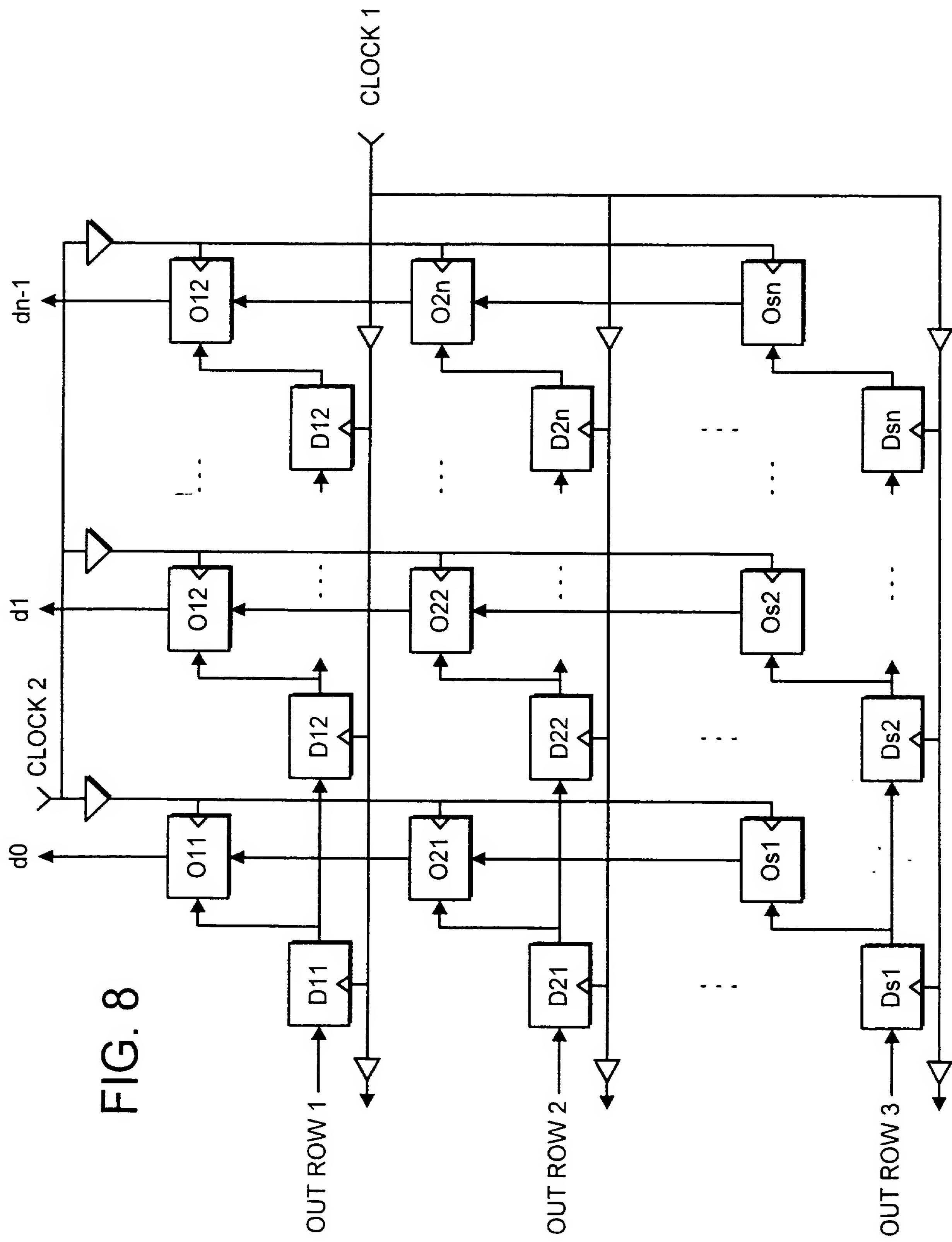


FIG. 7



IMAGING DEVICE FOR IMAGING RADIATION

This invention relates to an imaging device for imaging radiation, the imaging device comprising an array of image cells.

5 Imaging devices comprising an array of image cells of various types are known.

Charged coupled image sensors (also known as charged coupled devices (CCDs)) form one type of known imaging device. A CCD type device operates in the following way:

10 1. Charge is accumulated within a depletion region created by an applied voltage. For each pixel (image cell) the depletion region has a potential well shape and constrains electrons under an electrode gate to remain within the semiconductor substrate.

15 2. Voltage is applied as a pulse to the electrode gates of the CCD device to clock each charge package to an adjacent pixel cell. The charge remains inside the semiconductor substrate and is clocked through, pixel by pixel, to a common output.

During this process, additional charge cannot be accumulated.

Another type of imaging device which is known is a semiconductor pixel detector which comprises a semiconductor substrate with electrodes which apply 20 depletion voltage to each pixel position and define a charge collection volume. Typically, simple buffer circuits read out the electric signals when a photon is photo-absorbed or when ionising radiation crosses the depletion zone of the substrate. Accordingly pixel detectors of this type typically operate in a pulse mode, the numbers of hits being accumulated externally to the imaging device. The buffer 25 circuits can either be on the same substrate (EP-A-0,287,197) as the charge collection volumes, or on a separate substrate (EP-A-0,571,135) that is mechanically bonded to a substrate having the charge collection volumes in accordance with, for example, the well known bump-bonding technique.

A further type of device is described in International application WO95/33332. 30 In WO95/33332, an Active-pixel Semiconductor Imaging Device (ASID) is described. The ASID comprises an array of pixel cells including a semiconductor substrate having an array of pixel detectors and a further array of pixel circuits. The pixel

detectors generate charge in response to instant radiation. Each pixel circuit is associated with a respective pixel detector and accumulates charge resulting from radiation incident on the pixel detector. The pixel circuits are individually addressable and comprise circuitry which enables charge to be accumulated from a plurality of successive radiation hits on the respective pixel detectors. The device operates by accumulating charge on the gate, for example, of a transistor. Accordingly, analogue storage of the charge value is obtained. At a determined time, the charge from the pixel circuits can be read out and used to generate an image based on the analogue charge values stored in each of the pixel circuits.

CCD devices suffer from disadvantages of limited dynamic range, due to the limited capacity of the potential well inside the semiconductor substrate, and also to the inactive times during which an image is read out. Pulse counting semiconductive pixel devices also have the disadvantage of limited dynamic range. As these devices read the pixel contact when a hit is detected, they suffer from saturation problems at high counting rates. The semiconductor pixel device according to WO95/33332 provides significant advantages over the earlier prior art by providing a large dynamic range for the accumulation of images.

However, CCD imaging devices and imaging devices of the type described in WO95/33332 suffer from a potential disadvantage in that the output signals from the individual pixel cells represent the accumulation of radiation intensity at that pixel cell between readout times. This means that radiation hits of varying energies could lead to an inaccurate count of the number of radiation hits. For example, a relatively small number of higher energy radiation hits would give the same output signal as a higher number of lower energy radiation hits (for example scattered radiation hits).

The invention seeks to mitigate the problems of the prior art described above. In accordance with a first aspect of the invention there is provided an imaging device for imaging radiation comprising an imaging cell array including an array of detector cells which generate charge in response to incident radiation and an array of image cell circuits, each image cell circuit being associated with a respective detector cell, the image cell circuit comprising counting circuitry for counting plural radiation hits incident on the associated detector cell.

By counting each incident radiation hit on each image cell, it is possible to

provide an accurate count of the number of hits on each image cell even at high intensities (ie, high hit rates). An example of a device in accordance with the invention avoids readout bandwidth problems by counting at the image cells and allowing readout at a much lower rate than would be the case with typical pulse counting devices where the signals need to be read out of the device before being counted. The invention also simplifies the processing necessary on reading out the contents of the array of image cells. Typically the image cells will be pixels of a two dimensional array. However, the image cells could also be strips in a strip cell in an imaging strip device.

Preferably the image cell circuit comprises threshold circuitry connected to receive signals generated in the associated detector cell and having a values dependent on incident radiation energy, the counting circuitry being connected to the threshold circuitry for counting only radiation hits within a predetermined energy range or ranges.

By providing thresholding of the signals at each image cell, it is possible to reduce the storage capacity of the counter which is required, and also accurately to record the number of radiation hits of a desired energy. By recording hits of only selected radiation energies, it is possible for example to ensure that only directly incident rays are counted, and counting of hits resulting from scattered, reflected or defracted rays (which will have a lower energy) can be avoided. By use of this technique, the overall quality and resolution of an image can be greatly improved.

Preferably, the threshold circuitry comprises first and second comparators for comparing an input signal value to upper and lower threshold values, respectively. By using two comparators, it is possible to identify signals within a range having upper and lower bounds. With a single threshold comparator, it would be possible to obtain storage of signals either above, or below, that threshold.

In a first embodiment, a trigger circuit is responsive to outputs of the first and second comparators to increment a count in a counter in response to input signals having a value between the first and second threshold values. Preferably, this is achieved by providing the trigger circuitry with a flip-flop having a clock input connected via delay circuit to an output of the second comparator, a data signal input connected via a one shot circuit to an output of the first comparator and an output

connected to the counter.

To enable the image accumulation process to be substantially continuous, the output of the counter is connectable to a loadable shift register. The shift register of an image cell circuit is chained (in series) with respective shift registers of further 5 image cell circuits of the array.

In an alternative embodiment, a first counter is responsive to the output of the first comparator, and a second counter is responsive to an output of the second comparator. In order to enable the image accumulation process to be substantially continuous, in this embodiment the output of the first counter is connected to a first 10 loadable shift register and the output of the second counter is connected to a second loadable shift register. The first and second loadable shift registers of an image cell circuit are chained together (in series or possibly at least partially in parallel) and with shift registers of further image cell circuits of the array.

Preferably the shift registers of the image cell circuits are connected to an 15 output shift register arrangement external to the array. Preferably the output shift register has a dual x-y configuration.

The invention also provides an imaging system comprising an imaging device according to any one of the preceding claims.

Exemplary embodiments of the invention will be described hereinafter, by way 20 of example only, with reference to the accompanying drawings in which like elements have like reference signs and in which:

Figure 1 is a schematic block diagram of an overall imaging system configuration;

Figure 2 is a cross section of one example of a pixel imaging device;

25 Figure 3 is a schematic diagram of an image cell circuit of the image detector of Figure 2;

Figure 4 is a schematic block diagram of an example of threshold circuitry of the image cell circuit of Figure 3;

30 Figure 5 is a schematic block diagram of an example of counter circuitry of an image cell circuit of Figure 3;

Figure 6 is an alternative example of counter circuitry of an image cell circuit of Figure 3;

Figure 7 is a digital readout configuration for an array of image cell circuits; and

Figure 8 is a schematic block diagram of a dual x-y shift register.

Figure 1 is a schematic block diagram of one example of an imaging system
5 using an imaging device in accordance with the present invention. This particular embodiment is directed to the imaging of high energy radiation, for example X-ray radiation. By high energy radiation is meant radiation having an energy in excess of approximately 1 KeV. However, the invention is by no means limited to high energy radiation such as X-rays but could be applied to the detection of any particular
10 radiation , for example γ -ray, β -ray, α -ray , infra-red or optical radiation, subject to an appropriate choice of semiconductor substrate and threshold values as described later.

The imaging system 10 of Figure 1 is shown to provide imaging of an object 12 subject to radiation 14. In this example the radiation may, for example, be X-ray
15 radiation as mentioned above, but could alternatively be γ -ray, β -ray or α -ray radiation. The object 12 may, for example, be part of a human body. The imaging device 16 comprises a plurality of image cells (here pixel cells 18 of a two dimensional pixel array). In the following, reference will be made to pixel cells, although it will be appreciated that in other embodiments the individual image cells
20 may have a configuration other than that of a pixel within a two dimensional array (eg a strip arrangement).

The imaging device detects directly high energy incident radiation and accumulates at each pixel cell, a count of the incident radiation hits at that pixel cell.

The imaging device can be configured as a single semiconductor substrate (eg,
25 of silicon) with each pixel cell comprising a pixel detector 19 and a pixel circuit 20. Alternatively, the imaging device 16 can be configured on two substrates, one with an array of detector cells and one with an array of corresponding pixel circuits 20, the substrates being mechanically connected to each other by, for example, conventional bump-bonding technology or any other appropriate technology.

30 Figure 2 is a schematic cross section of part of an imaging device 16. In this example, the imaging device 16 comprises an image detector substrate 30 connected to an image circuit substrate 32 by means of bump-bonds 34. A pixel detector 19 of

each pixel cell 18 is defined on the detector substrate 30 by a continuous electrode 36 which applies a biasing voltage and pixel location electrodes 38 to define a detection zone for the pixel cell 18. Corresponding pixel circuits 20 on the image circuit substrate 32 are defined at locations corresponding to the electrodes 38 (ie to the pixel detectors 19). The pixel circuits 20 are electrically connected to the corresponding electrodes 38 by bump-bonds 34. In this manner, when charge is generated in a pixel detector 19 in response to incident radiation, this charge is passed via the bump-bond 34 to the corresponding pixel circuit 20.

The actual size of the pixel circuit and the pixel detector will depend on the application for which the imaging device is intended, and will also depend on the integrated circuit technology available for constructing the image circuit 20 to be described later. With current circuit technology, it is not possible to obtain the smallest possible image detectors which would be required in some applications. Typically, the minimum pixel size is of the order of 200 micrometres square using current technology. However, with advances expected in circuit manufacturing technology, it is expected that this minimum size can be significantly reduced using the teaching of the present application and improved circuit fabrication techniques. Accordingly, the present invention is not limited to any particular pixel image size.

As mentioned above, the pixel detectors and pixel circuits could be constructed integrally on a single semiconductor substrate. Such an implementation is possible, but sets challenges unrelated to the present invention, relating to circuit manufacturing techniques. With suitable circuit manufacturing techniques, the invention as described herein is perfectly applicable to implementation on a single semiconductor substrate, as opposed to the dual-substrate technique described herein.

Any appropriate semiconductor materials can be used for the substrates. For example, silicon may be used for the detector substrate and for the image circuit substrate. Other semiconductor materials could be used. For example, for the detector substrate, the material could be selected from: CdZnTe, CdTe, HgI₂, InSb, GaAs, Ge, TlBr, Si and PbI.

Figure 3 is a schematic diagram of an individual pixel circuit 20. The pixel detector 19 is represented by the diode in Figure 3. The input 50 to the pixel circuit 20 corresponds to the bump-bonding connection 34 between the pixel detector 19 and

the pixel circuit 20.

When a photon is photo-absorbed in a detection zone of the pixel detector 19 creating an electric charge, or when a charge radiation ionises a detection zone of the pixel detector 19, an electric pulse flows from the pixel detector 19 via the bump-bond 34/50 to threshold circuitry 42 of the pixel circuit 20. The threshold circuitry 42 effectively filters the input radiation intensity by comparing the input pulse peak to one or more threshold values. The output of the threshold circuitry 42 is connected to counter circuitry 44 for counting pulses (radiation hits) within one or more predetermined ranges as defined by the threshold circuitry. The counter circuitry is connected to counter circuitry of other (typically adjacent) pixel circuits for readout purposes. Various inputs to the pixel circuit 20 include hold 52, load 54, enable 56, reset 58 and clock 92 signal lines and voltage supply lines Vdd and Vss (not shown).

Figure 4 is a schematic block diagram of the threshold circuitry 42 represented in Figure 3. As shown in Figure 4, protection circuitry 60 is connected to the input node 50 (ie the bump-bond connection 34 to the pixel detector 19). The protection circuitry is provided to prevent damage due to over- or under-voltage values and is typically provided by two diodes connected to the high and low supply line Vdd and Vss (not shown). The output of the protection circuitry 60 is connected to amplifier/shaper circuitry 62 which produces an analogue signal proportional to the charge injection of a delta peak. Preferably, the amplifier shaper 62 is implemented by means of a charge sensitive amplifier followed by a shaper. The shaping time depends on the maximum signal rate on a pixel. Figure 4 illustrates optional baseline subtraction circuitry which is needed if the leakage current varies significantly within the selected shaping time. Optionally, one can select the time when the baseline is sampled. In this case, the baseline is sampled outside normal measurement times.

A differential amplifier 66 subtracts the baseline so that comparators 68 and 70 see the true peak signal height. First and second comparators 68 and 70 have respective high and low threshold values 72 and 74 input thereto. The high and low threshold values can represent higher and lower limits of accepted signal amplitudes. In this case any signal peaks below the low threshold and above the high threshold will be rejected by the counter circuitry 44. If the peak signal value exceeds the high

threshold value 72, then the first comparator 68 outputs a logic 1, otherwise it outputs a logic 0.

Similarly, if the peak signal value exceeds the low threshold value 74, then the second comparator 70 outputs a logic 1, otherwise it outputs a logic 0. It will be
5 appreciated that the comparison output values of the present embodiment form one example only and in other embodiments of the invention other values could be output as a result of the comparisons.

Figure 5 is a schematic block diagram of a first example of counter circuitry
44. Depending on the shaping parameters and signal amplitudes, the high output
10 signal 76 from the first comparator 68 always comes some time later than the low output 78 from the second comparator 70. In Figure 5, the high output 76 from the first comparator 68 is supplied to a one shot circuit 80 which is responsive to the enable signal 56. The low output 78 from the second comparator 70 is supplied to a delay circuit 82. By applying a delay to the low output 78, the order of the signals
15 76 and 78 can be reversed so that the signal received from the delay circuit 82 at the clock input C of a D-flip-flop 84 always comes later than the inverted output of the one-shot circuit 80 which is supplied to the D input of the flip-flop 84. If the high threshold 72 was not exceeded by the input signal, the output Q of the flip-flop 84 will be set high. The output Q of the flip-flop 84 is connected via a delay 86 to a
20 reset input RESET of the flip-flop 84 to cause the flip-flop to be reset after a delay D2 to ensure a minimum pulse length for the output "clk" signal from the Q output of the flip-flop 84. An alternative to feeding back the output Q to the delay 86 is represented by the dotted line 85 from the delay circuit 82. Although a D-flip-flop
25 84 is shown in Figure 5, another type of flip-flop could be used.

The length of the single-triggered one-shot circuit 80 is adequate to coincide with the rising edge from the low output signal 78 from the second comparator 70 at all signal amplitudes.

The output "clk" from the output Q of the flip-flop 84 is provided as an input to an asynchronous n-bit counter 88. Accordingly to the type of counter used,
30 counting can be disabled with an enable signal 56 before latching an n-bit output from the counter 88 to a loadable shift register 90. The counter 88 can then be reset and the counter 88 can be enabled to proceed with counting. Reading from the pixel

circuit can then be effected during the next counting period in response to the clock signal 92.

The overall operation of the triggered counter arrangement shown in Figure 5 is to cause a count to be accumulated in the counter 88 on each occasion that a signal is received in response to a radiation hit having an energy between the high and low threshold values 72 and 74.

An alternative arrangement for the counter circuitry is illustrated in Figure 6. In the alternative counter circuitry shown in Figure 6, both low and high output counts are directly obtained. This circuitry requires more circuit real estate and readout time than the circuitry of Figure 5, but it does allow a direct readout of the number of counts between the thresholds by subtracting the low count from the high count and also allows the output of the number of the counts higher than the high threshold by counting the high count only.

In Figure 6, therefore, an asynchronous n-bit counter 94 is connected directly to receive the high output of the first comparator 68. An asynchronous n-bit counter 96 is connected directly to receive the output 78 of the second comparator 70. In response to load signals 54, first and second loadable shift registers 98 and 100 can be loaded with the contents of the first and second asynchronous n-bit counters 94 and 96, respectively. As with the previous example, the contents of the loadable shift registers 98 and 100 can be read out in response to a clock signal 92 during a subsequent counting period.

Figure 7 is a schematic block diagram representing a two dimensional array of image cells (an array of pixel cells) having r columns and s rows. The r*s pixel cells are connected to a control logic block which generates the load, reset, enable, hold and the threshold signals which are common to all pixels. Some of the signals may in fact be the same. Preferably the high and low threshold values are adjustable to enable the desired energy range for accepted radiation hits to be varied. The control logic block can receive the Vdd and Vss supply voltages and to supply these voltages further to the pixel array 32 and the shift register 104. The loadable shift registers 90 or 98 and 100 of a row of individual pixel cells are chained together so that a serial input 46 of a loadable shift register 90 or 98 of one pixel circuit is connected to the serial output 48 of a loadable shift register 90 or 100 of a

neighbouring pixel circuit. In this way, the output from the individual pixel cells are chained together so as to form one long shift register (in this example, one shift register per row) which is connected to an n-bit (or $2*n$ -bits in a second set up) shift register 104. This register has a dual x-y storage capacity so that it can output 5 rapidly s rows of n-bit ($2*n$) data. The clock for each pixel cell is distributed via the shift register 104 to ensure the same delay paths for each row of the pixel array on the semiconductor substrate.

Figure 8 represents the shift register 104 of Figure 7 in more detail. This shift register has a dual x-y configuration formed from a horizontal shift register 10 10 (stages D_{xy}) and a fast vertical loadable shift register (stages O_{xy}). Each bit from the respective rows of the pixel array are loaded simultaneously to the vertical register after all bits ($n/2*n$) have been clocked out for a single pixel cell. After that, the next pixel cell can be read out while the previous s rows of data have been read out vertically. It should be noted that the common load signal for the vertical shift 15 registers marked O_{xy} has not been illustrated in Figure 8.

Returning to Figure 1, it will be appreciated that the control electronics 24 comprises a combination of the control logic 102 and the shift register arrangement 104. The control electronics 24 is connected by a path represented schematically by the arrow 26 to an image processor 28. Thus, the data output from the shift register 20 104 can be supplied to the image processor 28. The image processor 28 includes data storage in which it accumulates digital values representative of the number of hits on the respective pixels of the pixel array and identifies the position of each pixel within the array. As a result, each image can be stored as a representation of a two-dimensional array of pixel values. The two-dimensional array can be stored by means 25 of any appropriate database.

The image processor 28 accesses stored image data in the database to select a given image (all of the array) or part of the image (a subsample of the image array). The image processor reads the value stored for the selected pixel positions and causes a representation of the data to be displayed on a display 32 via a path 30 represented schematically by the arrow 30. The data can of course be printed rather than, or in addition to being displayed, and can be subjected to further processing operations. Background and noise can be subtracted as a constant from each pixel

charge value. This pedestal and/or background subtraction is possible if prior to image taking an "empty image" is acquired. For each pixel a background value is deduced and can be subtracted accordingly. In order to control the operation of the image processor and the display, input devices 36, for example a keyboard, pointing device, etc, can be provided.

There has been described an imaging device and imaging system which enables accurate counts of the number of radiation hits on a particular image cell of an image array. An example of the invention enables the advantages of an accumulation type imaging device such as described in WO95/33332 to be achieved, with the added advantage that, rather than accumulating a charge value for incident pixels on the array during an accumulation period, the number of actual hits is recorded at each pixel cell of the pixel array. This provides highly accurate imaging while still permitting fast readout with little or no "dead time" associated with readout. With the preferred provision of thresholding circuitry on each pixel cell, the pixel circuit can be arranged to count only those radiation hits within desired incident energy parameters. As a result of this, the input device can be tuned to select only image radiation having desired energy values or ranges. An imaging device in accordance with this preferred feature of the present invention thus enables scattered radiation to be eliminated and only directly incident radiation to be counted. The use of the threshold circuitry on the individual pixel circuits of a device in accordance with the present invention enables the advantages of imaging devices such as are described in WO95/33332 to be achieved with further advantages of accurate counts of incident rays on each pixel and discrimination of incident ray energy at each pixel circuit.

Although particular embodiments of the invention have been described, it will be appreciated that the invention is not limited to those embodiments, and many modifications are possible within the scope of the present invention. Thus, although a particular combination of threshold and counter circuitry has been described, other embodiments are possible within the scope of the invention.

For example, in the described embodiment the high and low threshold values are supplied from the control logic 102 and are preferably adjustable. However in alternative embodiments the high and low threshold values could be derived from the

Vdd and Vss supply voltages in a fixed manner.

Optionally, if desired, an analogue signal representative of the incident energy of a radiation hit can be taken at 106 (dotted line) from the differential amplifier 66 (see Fig 4). This analogue signal could then be accumulated in charge storage means 5 (eg, in a transistor or capacitor) to give a value representative of the total energy incident on a pixel detector from the last reset of the charge storage means.

CLAIMS

1. An imaging device for imaging radiation comprising an image cell array including an array of detector cells which generate charge in response to incident radiation and an array of image cell circuits, each image cell circuit being associated with a respective detector cell, said image cell circuit comprising counting circuitry for counting plural radiation hits incident on said associated detector cell.
5
2. An imaging device according to Claim 1, wherein said image cell circuit comprises threshold circuitry connected to receive signals generated in said associated detector cell and having values dependent on incident radiation energy, said counting circuitry being connected to said threshold circuitry for counting only radiation hits within a predetermined energy range or ranges.
10
3. An imaging device according to Claim 2, wherein said threshold circuitry comprises first and second comparators for comparing an input signal value to upper and lower threshold values, respectively.
15
4. An imaging device according to Claim 3, wherein said counting circuitry counts radiation hits having an energy which generates an input signal value between said first and second threshold values.
20
5. An imaging device according to Claim 4, wherein said counting circuitry comprises trigger circuitry responsive to outputs of said first and second comparators to increment a count in a counter in response to input signals having a value between said first and second threshold values.
25
6. An imaging device according to Claim 5, wherein said trigger circuitry comprises a flip-flop having a clock input connected via a delay circuit to an output of said second comparator, a data signal input connected via a one-shot circuit to an output of said first comparator, and an output connected to said counter.
30
7. An imaging device according to Claim 6, wherein said output of said counter

is connected to a loadable shift register, said shift register of an image cell circuit being chained with respective shift registers of further image cell circuits of said array.

5 8. An imaging device according to Claim 4, comprising a first counter responsive to an output of said first comparator, a second counter responsive to an output of said second comparator.

9. An imaging device according to Claim 8, wherein an output of said first
10 counter is connected to a first loadable shift register, and said output of said second counter is connected to a second loadable shift register, said first and second loadable shift registers of an image cell circuit being chained together and with respective shift registers of further image cell circuits of said array.

15 10. An imaging device according to Claim 7 or Claim 9, wherein said shift registers of said image cell circuits are connected to an output shift register arrangement external to said array.

11. An imaging device according to Claim 10, wherein said output shift register
20 comprises dual x-y configuration.

12. An imaging device according to any preceding Claim, wherein said image cell array is a pixel cell array.

25 13. An imaging system comprising an imaging device according to any preceding Claim.

14. An imaging device substantially as hereinbefore described with reference to the accompanying drawings.

30

15. An imaging system substantially as hereinbefore described with reference to the accompanying drawings.



The
Patent
Office

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Claims searched: All

Examiner: James Porter
Date of search: 12 February 1997

Patents Act 1977
Search Report under Section 17

Databases searched:

UK Patent Office collections, including GB, EP, WO & US patent specifications, in:

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Int Cl (Ed.6): G01T 1/161, 1/164, 1/20, 1/24; H04N 5/335

Other: Online database: WPI

Documents considered to be relevant:

Category	Identity of document and relevant passage	Relevant to claims
X	EP0205624 A1 (NIPPON) See whole document	1
A	WO95/33332 A2 (SIMAGE OY)	-
X	WPI Abstract Accession No. 87-274543/39 & JP62191787 A (MATSUSHITA) 22.08.87 See abstract and figure.	1, 2

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Y Document indicating lack of inventive step if combined with one or more other documents of same category.
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